Abstracts

A robust high voltage Si LDMOS model extraction process to achieve first pass linear RFIC amplifier design success (2002 [RFIC])

J.A. Pla and D. Bridges. "A robust high voltage Si LDMOS model extraction process to achieve first pass linear RFIC amplifier design success (2002 [RFIC])." 2002 Radio Frequency Integrated Circuits (RFIC) Symposium 02. (2002 [RFIC]): 347-350.

A robust model extraction procedure was developed for a high voltage Si LDMOS RFIC process to achieve first pass linear RFIC amplifier design success. The model extraction process utilizes pulsed isothermal small-signal S-parameter measurements and extracted large-signal Root Models at three different temperatures to extract model parameters for Motorola's Electro-Thermal (MET) FET analytical model. Large-signal model validation was performed against loadpull measurements under 1-tone and 2-tone stimuli. Also, the models were developed into a design kit within Agilent/sup (R)/ EEsof/sup (R)/'s ADS/sup (R)/ (Advanced Design System) to design a wide-band 30 Watt power amplifier IC which achieved first pass design success.

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